FPGA-Based LED Display

Komal Shah1, Aashita Irani2 and Nikhil Gala3

1,2,3 SVKM’s NMIMS University’s, Mukesh Patel School of Technology Management and Engineering (MPSTME), Department of Electronics and Telecommunication, Behind Homeopathy College, Bhakti VedantaSwami Marg, JVPD Scheme, Vile-Parle (West), Mumbai - 400 056, India.

1kkshah789@gmail.com, 2aashitaairani@yahoo.co.in and 3nikhilgala@hotmail.com

ABSTRACT
The following paper suggests a design for FPGA based low cost LED display board. Roughly tens of thousands of large-size LED display boards have been installed worldwide. The adoption of LED display boards can become even more widespread if the overall system price can be significantly reduced and the operational procedure of such display boards can be simplified. In the following paper, we propose a new architecture which uses a combination of an inexpensive FPGA chip and LED driver to build a LED display. Thus, representing design for a basic, low cost, modular LED video-display board.

KEYWORDS
LED display matrix, Low cost FPGA, LED driver, DVI receiver.

1. INTRODUCTION
Display technology pervades all aspects of present day life, from televisions to automobile and from dashboards to billboards on high roads. Single colored LED display boards are very common now-a-days. The same yellow or red colored board is not attractive. The introduction of multicolored LEDs into the display boards make them attractive. This project is oriented towards the development of a prototype of a multicolored LED display board which is being controlled by a LED driver. The fundamental part is a 4X4 LED module which could be repeated column wise or row wise to enlarge the display without any change in circuitry. The proposed design uses Field Programmable Gate Array (FPGA) which is an integrated circuit designed to be configured by the circuit designer, after manufacturing. The ability to update the functionality at later stage, partial re-configuration of the portion of the design and the low non-recurring engineering costs offer advantages for display technologies. The design also employs LED driver and DVI receiver, for controlling the display board and interfacing with the computer, respectively. Motivation towards the project was to make available a readily expandable multicolor display board which can be used for multiple purposes.

2. ARCHITECTURE

2.1. DVI RECEIVER
Data transfer from PC to FPGA is done through serial communication using Transition Minimized Differential Signaling (TMDS) technology for high-speed serial data transfer. The transmitter incorporates an advanced coding algorithm which reduces electromagnetic interference over copper cables and enables robust clock recovery at the receiver to achieve high skew tolerance for driving longer cables as well as shorter low cost cables. Digital Visual Interface (DVI) compliant TMDS (Transition Minimized Differential Signaling) digital receiver is used to receive and decode TMDS encoded RGB pixel data streams from the host (such as personal computer). We propose utility of DVI Receiver TFP401 by Texas Instruments [2]. In the design of digital display system, the host, a PC or workstation, contains a TMDS compatible transmitter that receives 24 bit pixel data along with appropriate control signals and encodes them into a high-speed low-voltage differential serial bit stream fit for transmission over a twisted-pair cable. This decoded data is then applied directly to the display controlling circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred.

2.2. FPGA BOARD
Field Programmable logic is one of the most rapidly evolving digital electronics technology areas and expectations for future integration with digital system-on-chip design are high. The benefit is availability of more flexible devices, which have longer life-span then those, designed with rigid hardware boundary in mind. Thus FPGA is considered for the design of this LED display board. FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be connected together, like an on-chip programmable breadboard. Logic blocks can thus also be configured to perform complex combinational functions. The logic blocks include memory elements, which aids in implementing the necessary memory scanning and video signal timing. Thus FPGA provides control over every single LED of the display. Various features of the display such as contrast, brightness, etc. can also be controlled through user interface at PC. This data from PC is transferred to LED driver through FPGA. FPGA chip proposed for this design is Altera EP2C20 QPFP [4], which is a 240 pin integrated circuit. The integrated circuit contains many identical logic cells that can be viewed as standard components. The individual cells are interconnected by a matrix of wires and programmable switches. The FPGA can be programmed through local serial EPROM. The FPGA can also be programmed by downloading the entire program into the FPGA from the IP bus for those applications that require complete security.

2.3. LED DRIVER

LEDs are current-driven devices whose brightness is proportional to their forward current. Forward current can be controlled in two ways. The first method is to use the LED Voltage-Current curve to determine what voltage needs to be applied to the LED to generate the desired forward current. However, this method has several drawbacks. Such as any change in LED forward voltage creates a change in LED current. The second, preferred method of regulating LED current is to drive the LED with a constant-current source. The constant-current source eliminates changes in current due to variations in forward voltage, which translates into a constant LED brightness. This functionality is provided by LED driver [3]. We propose the usage MAX6794, LED driver by Maxim [1]. The MAX6794 is available in 40-pin TQFN packages and operates over -40°C to +125°C temperature range. The MAX6794 operate from a 3.0V to 3.6V power supply. The full-scale current for each bank of eight outputs is adjustable from 6mA to 30mA. An internal watchdog timer, when a fault is detected and the accumulated count value returns to the hardware. Thus FPGA is considered for the design of this LED display board. FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be connected together, like an on-chip programmable breadboard. Logic blocks can thus also be configured to perform complex combinational functions. The logic blocks include memory elements, which aids in implementing the necessary memory scanning and video signal timing. Thus FPGA provides control over every single LED of the display. Various features of the display such as contrast, brightness, etc. can also be controlled through user interface at PC. This data from PC is transferred to LED driver through FPGA. FPGA chip proposed for this design is Altera EP2C20 QPFP [4], which is a 240 pin integrated circuit. The integrated circuit contains many identical logic cells that can be viewed as standard components. The individual cells are interconnected by a matrix of wires and programmable switches. The FPGA can be programmed through local serial EPROM. The FPGA can also be programmed by downloading the entire program into the FPGA from the IP bus for those applications that require complete security.

PWM control: The driver provides 12-bit individual PWM steps for each LED output, providing fine resolution adjustment of average current output. LED intensity control: The driver provides three levels of output current control for driving LED- individual intensity control, global-intensity control and calibration DACs (CALDACs)

- a. The individual intensity control- it operates on each output independently to set each individual LED intensity level.
- b. The global-intensity control- it modulates outputs simultaneously for a uniform brightness control without affecting color. Finally, all outputs can be turned on and off simultaneously by setting or clearing configuration bit D3 (PWM-ON).
- c. Calibration Digital to Analog Converter (CALDAC) control- The 8-bit R, G, and B CALDACs set the output current level for all eight outputs in the R, G, and B ports, respectively. The R CALDAC, G CALDAC, and B CALDAC range from a low of 6mA to a maximum of 30mA. The B CALDAC data is loaded first, followed by the G CALDAC data, and then the R CALDAC data.

Serial-Interface Protocol Structure: The MAX6974 serial interface transfers all data and control functions using a protocol structure consisting of header and data segments transmitted in specific sequence.

Header Segment

The 24-bit header segment consists of an 8-bit fixed synchronization pattern (SYNC), a 6-bit command pattern (CMD), and a 10-bit counter (CNTR) segment.

<table>
<thead>
<tr>
<th>HDR</th>
<th>CMD</th>
<th>CNTR</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>02</td>
<td>03</td>
</tr>
<tr>
<td>04</td>
<td>05</td>
<td>06</td>
</tr>
<tr>
<td>07</td>
<td>08</td>
<td>09</td>
</tr>
<tr>
<td>10</td>
<td>11</td>
<td>12</td>
</tr>
<tr>
<td>13</td>
<td>14</td>
<td>15</td>
</tr>
</tbody>
</table>

**Table 1:** Serial interface header

SYNC- Synchronization bit pattern 0xE8 is recognized by the driver during intervals when LOADI is low.

CMD- Send command bits C1 and C0 three times in succession. The command bits define how many data bits are received and where the data is loaded. The four commands are:

- 00: Load individual PWM
- 01: Load CALDAC
- 10: Load global-intensity PDM
- 11: Load configuration

**Table 2:** Command bits

CNTR- This is the counter for open LED or over temperature fault conditions. The host sends the header segment with the counter value set to zero. The counter value is incremented when a fault is detected and the accumulated count value returns to the host.
CMD = X0 Over temperature faults counted
CMD = X1 Open LED faults counted

Data Segment
The bit length of the data segment received by the MAX6974 is dependent on the command specified in the header. The data is always organized as B driver data first in the order of B7 first to B0 last (MSB first), followed by the G driver data in the same order of G7 to G0 (MSB first), and then the R driver data in the order of R7 to R0 (MSB first).

2.4 LED MATRIX

<table>
<thead>
<tr>
<th>R1</th>
<th>G1</th>
<th>B1</th>
<th>R2</th>
<th>G2</th>
<th>B2</th>
<th>R3</th>
<th>G3</th>
<th>B3</th>
<th>R4</th>
<th>G4</th>
<th>B4</th>
</tr>
</thead>
<tbody>
<tr>
<td>R5</td>
<td>G5</td>
<td>B5</td>
<td>R6</td>
<td>G6</td>
<td>B6</td>
<td>R7</td>
<td>G7</td>
<td>B7</td>
<td>R8</td>
<td>G8</td>
<td>B8</td>
</tr>
<tr>
<td>R14</td>
<td>G14</td>
<td>B14</td>
<td>R15</td>
<td>G15</td>
<td>B15</td>
<td>R16</td>
<td>G16</td>
<td>B16</td>
<td>R17</td>
<td>G17</td>
<td>B17</td>
</tr>
</tbody>
</table>

Fig. 2: LED matrix

The matrix used for this design is a 4x4 LED matrix where Red, Green and Blue are arranged as shown in the above figure. There are 16 Red, Green and Blue LEDs each, thus making the total number of LED count to 48. This is possible since the driver is operating in the multiplex mode. Hence there are two Red LEDs connected at one Red output drive pin of MAX6794. Thus each output drive pin has capability of driving two LEDs. The LED power supply can range from 3V to 7V. In multiplexed mode the LEDs are connected to a pnp transistor too, as shown in the figure.

2.6 DRAWBACKS
1. The computer controlled large size display may find the connections of display with the computer difficult
2. The increase in number of LEDs require more number of LED drivers
3. The high resolution video graphics and images will not be justifiably displayed on the LED display

3. CONCLUSION AND FUTURE SCOPE
Thus the design can provide a way to design a low cost FPGA based LED display. The future applications may include:
1. The display features can be extended for video display using a PC card.
2. Triple output LEDs which can provide Red, Green and Blue output light from a single LED can be used for display.

REFERENCES
[3]. Embedded system design with C8051- by Han-Way Huang

2.5 BENEFITS
1. Low power consumption
2. Easily expandable in dimensions
3. More life span
4. LEDs doesn’t contain mercury and are not considered hazardous waste